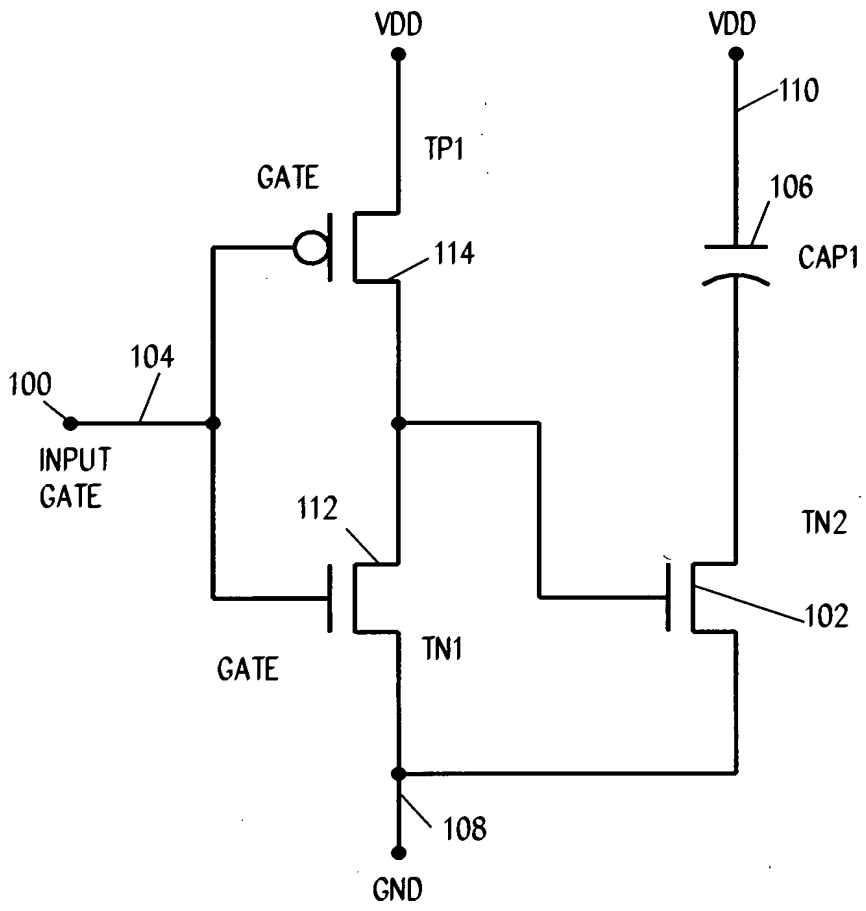
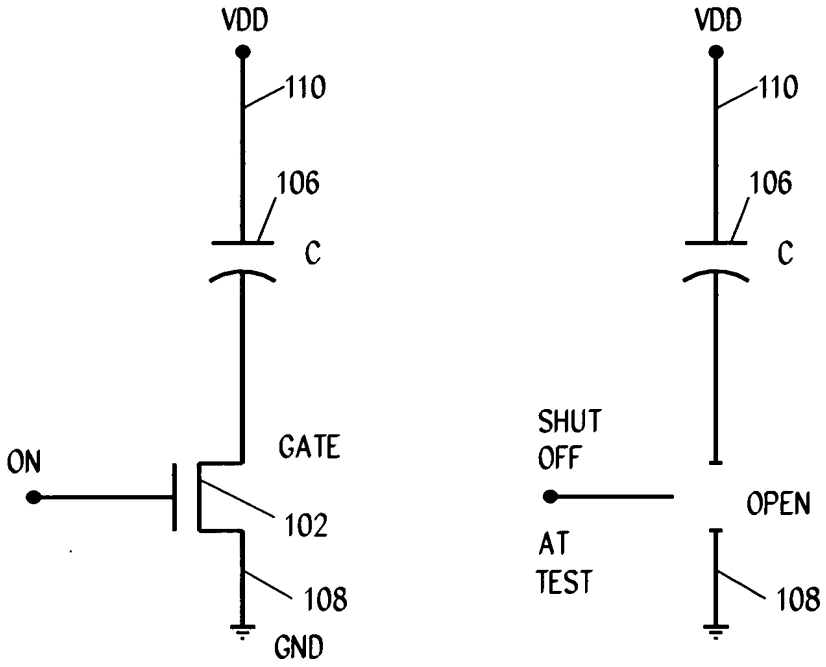


DECOUPLING CAP WITH NFET GATE

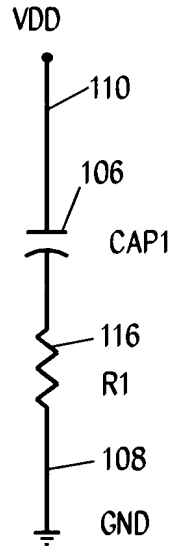
PRIOR ART

FIG. 1



PRIOR ART

FIG. 2



PRIOR ART

FIG. 3

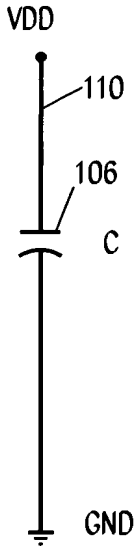
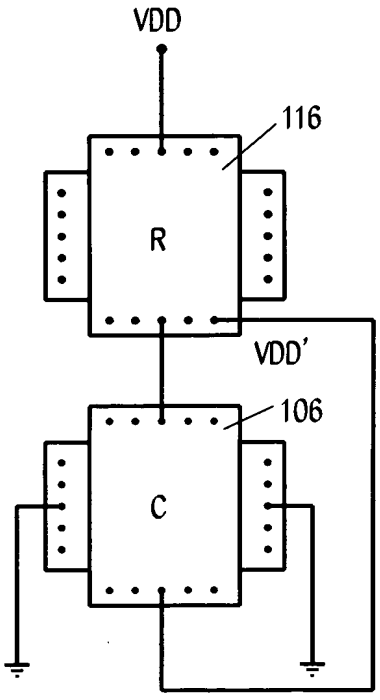


FIG. 5

DECOUPLING CAP WITH
INTEGRATED RESISTOR



PRIOR ART

FIG. 4

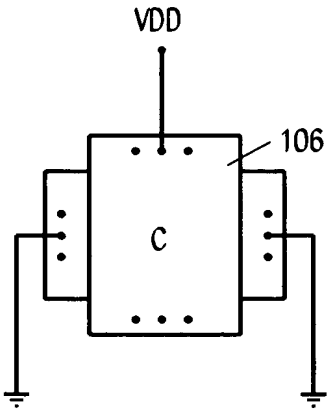


FIG. 6

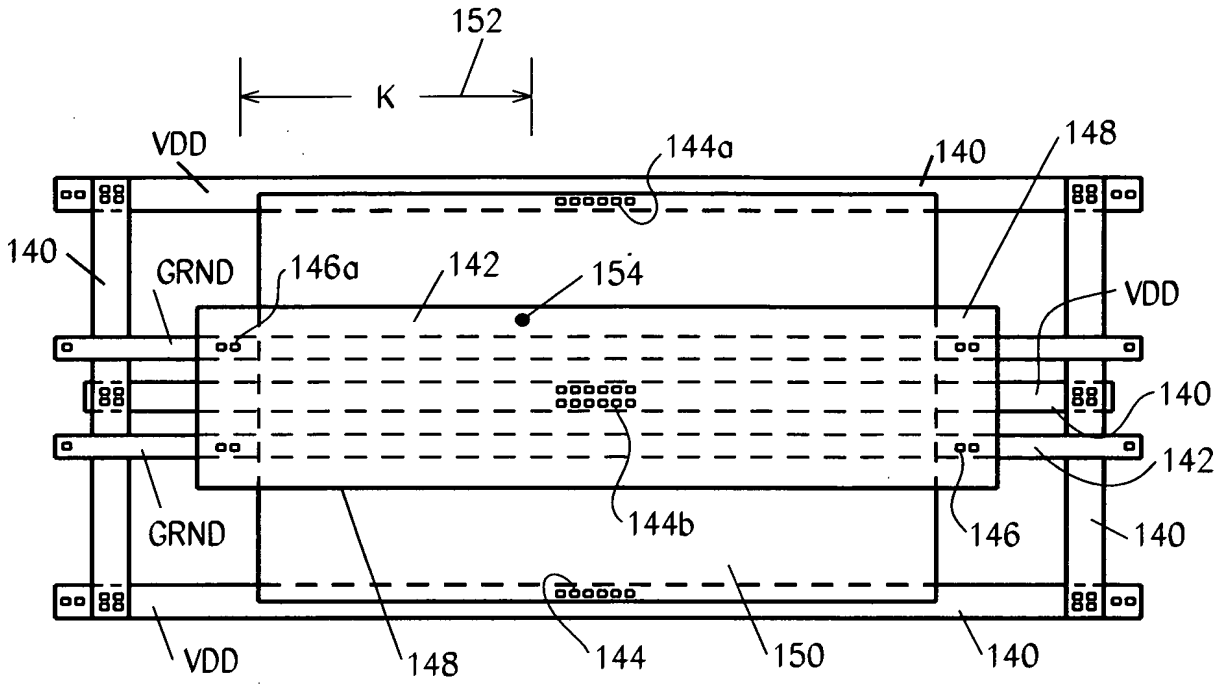

152
K
VDD
144a
140
148
140
GRND
146a
142
154
VDD
140
142
GRND
144b
146
140
VDD
148
144
150
140

FIG. 7

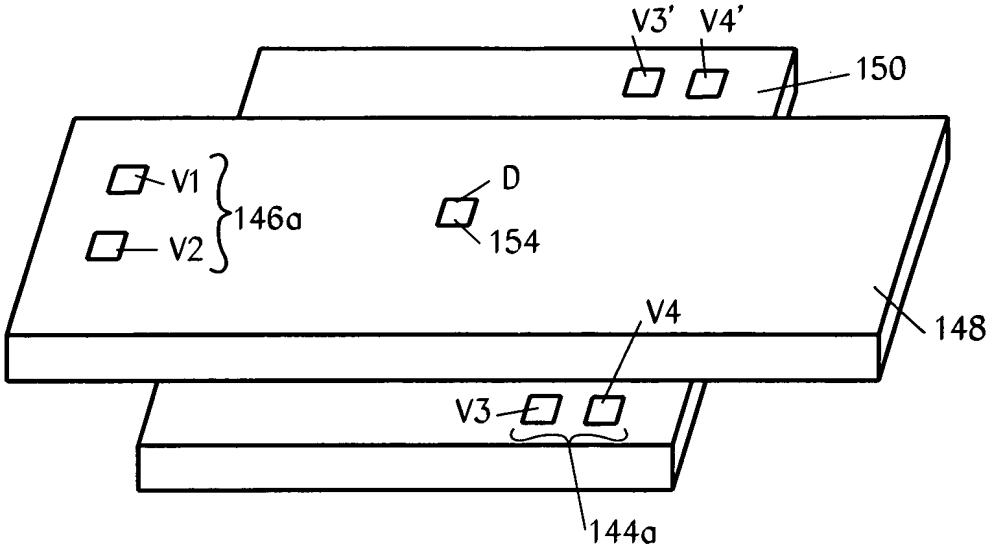

V3'
V4'
150
V1
V2
146a
D
154
V4
148
V3
144a

FIG. 8

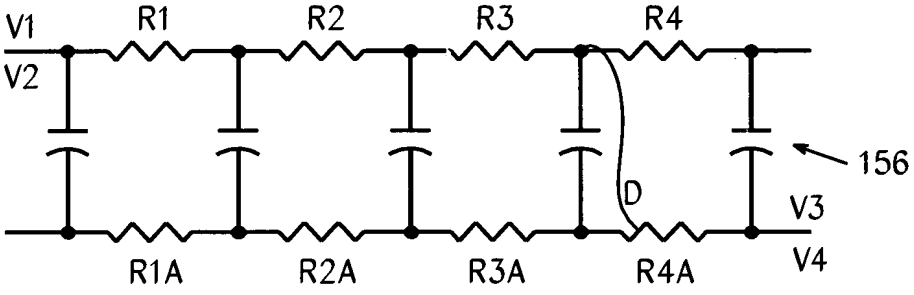

V1
V2
R1
R2
R3
R4
156
D
V3
V4
R1A
R2A
R3A
R4A

FIG. 9

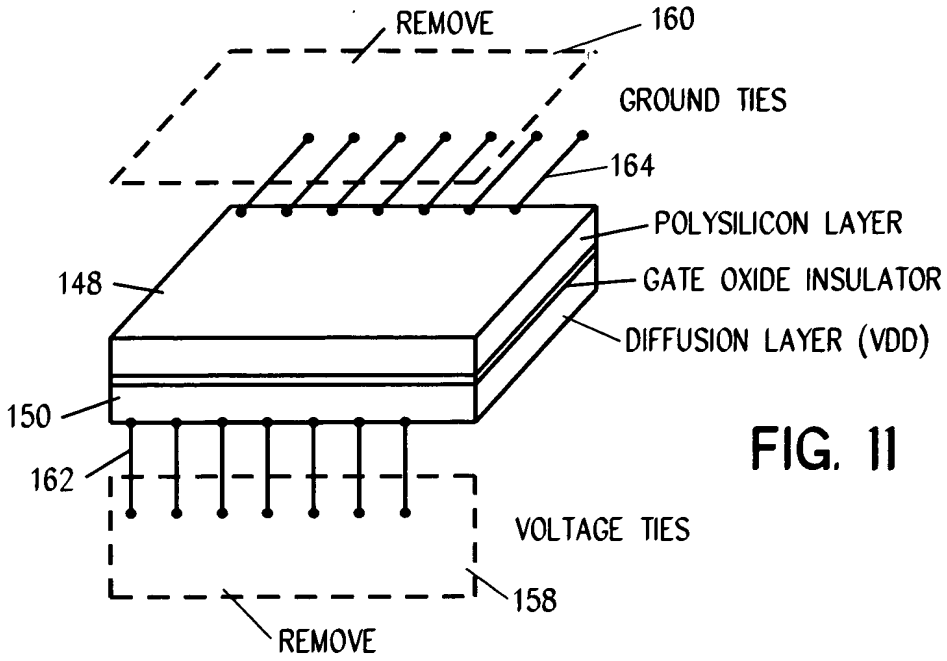


FIG. 11

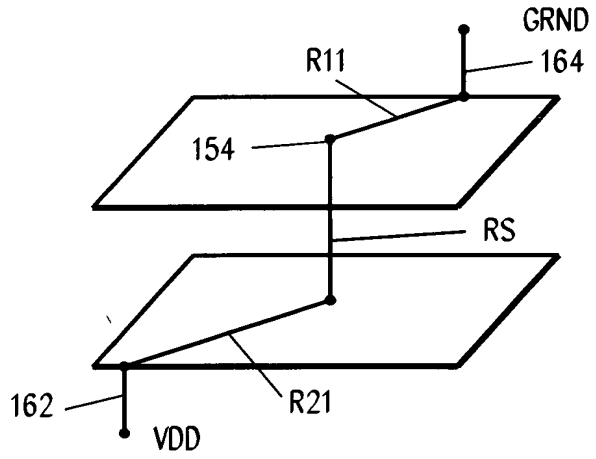


FIG. 12

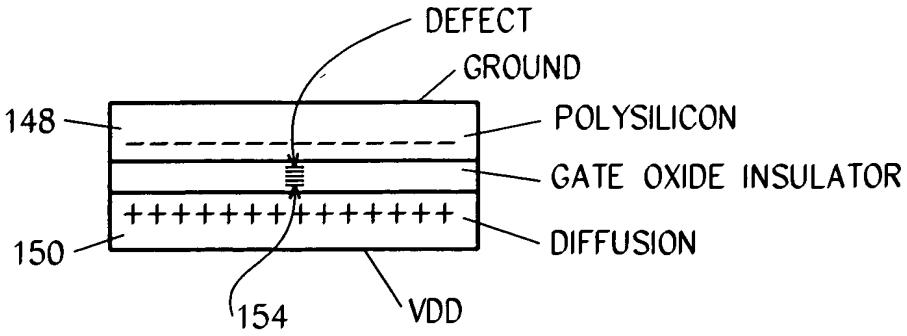


FIG. 10

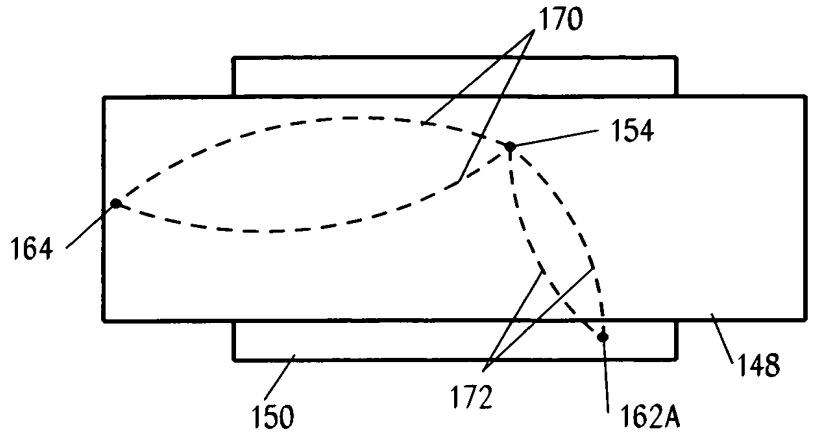


FIG. 13

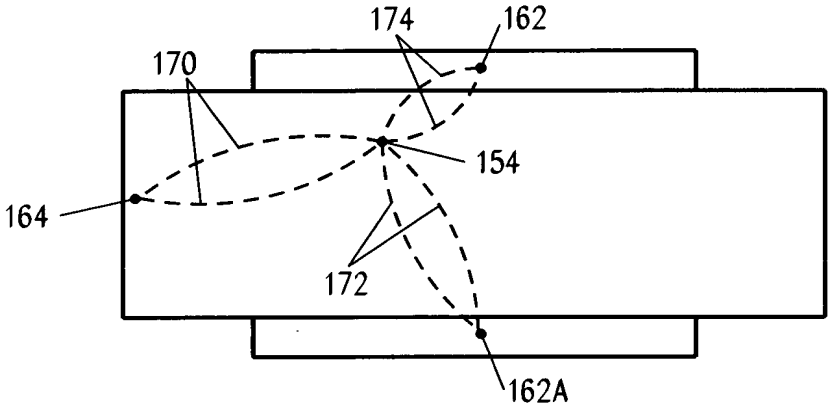


FIG. 14

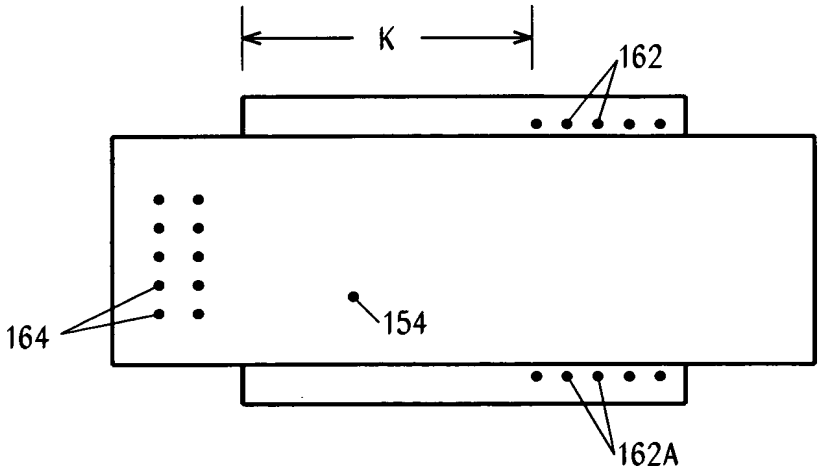


FIG. 15

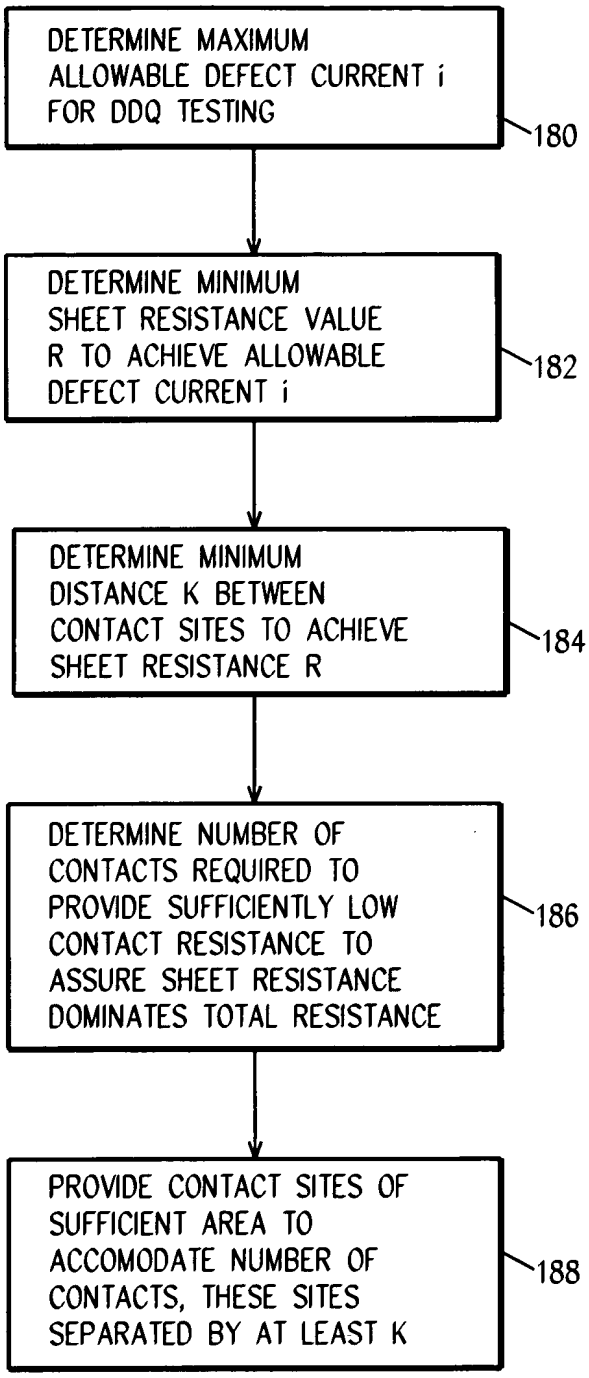

DETERMINE MAXIMUM ALLOWABLE DEFECT CURRENT i FOR DDQ TESTING
180
DETERMINE MINIMUM SHEET RESISTANCE VALUE R TO ACHIEVE ALLOWABLE DEFECT CURRENT i
182
DETERMINE MINIMUM DISTANCE K BETWEEN CONTACT SITES TO ACHIEVE SHEET RESISTANCE R
184
DETERMINE NUMBER OF CONTACTS REQUIRED TO PROVIDE SUFFICIENTLY LOW CONTACT RESISTANCE TO ASSURE SHEET RESISTANCE DOMINATES TOTAL RESISTANCE
186
PROVIDE CONTACT SITES OF SUFFICIENT AREA TO ACCOMODATE NUMBER OF CONTACTS, THESE SITES SEPARATED BY AT LEAST K
188

FIG. 16

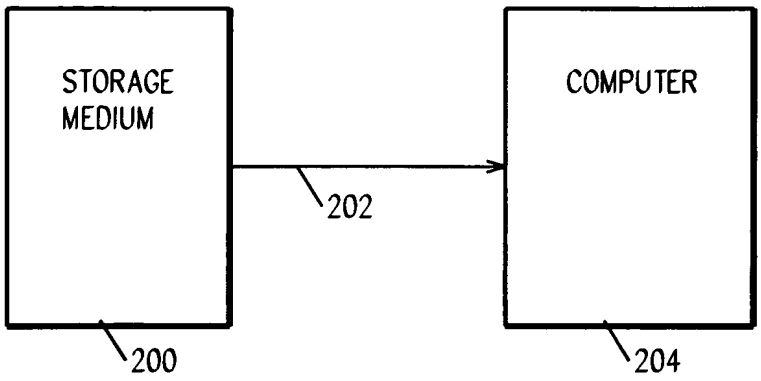


FIG. 17